ABSTRACT OF THE DISCLOSURE

In a display device of the present invention, during a period until the start of outputting display data from a source driver, a timing control ASIC generates a gate start pulse signal GSP and a first pulse CK1 of a gate clock signal GCK, with reference to the timing of inputting a data enable signal ENAB. The signals having been generated are supplied to the gate driver, so that a dummy line G0 is driven.